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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,235	09/17/2003	Krishna M. Desai	POU920020104US1	6995

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,235	DESAI ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-13* is/are rejected.

7)☒ Claim(s) *7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are presented for examination.

2. The IDS filed on 09/17/2003 has been received and carefully considered.

Claim Objections

3. Claims 8 and 12 are objected to because of the following informalities:

The difference between the first and second operation modes is not clearly claimed in the claim 8 of this application. Lines 4-13 of claim 8 claims that in both the first and second operational modes, both the cache directory and cache array are updated regardless of a cache hit or a cache miss.

The phrase should be "said address bits" instead of "said by address bits" as disclosed in claim 12 of this application.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishimi et al. (USPN: 5,708,803) hereinafter, Ishimi.

As per claim 8, Ishimi teaches a system of writing to cache comprising: a cache directory (the tag unit 2 in Fig. 3); a cache array (the data unit 3 in Fig. 3); control logic (i.e. the valid bit unit 90 in Fig. 3) for writing a valid field (i.e. a valid bit) and an address to said cache directory and data to said cache array. As described above under the Claim Objection heading, in both the first and second operational modes, both the cache directory and cache array are updated regardless of a cache hit or a cache miss. Ishimi discloses these limitations at Col. 5, lines 14-17: when a cache miss occurs, external data bus is accessed and the data is fetched, i.e. from the further storage/memory; and when the cache hit occurs, the data is accessed from the cache. Similarly, in the normal cache operating mode, when the cache miss occurs, the data is written both in cache memory and the further storage/memory; and when the cache hit occurs, the data is updated only in the cache memory (e.g. see Col. 12, lines 40-43; Col. 13, lines 24-32 and Col. 5, lines 14-17).

As per claim 9, Ishimi teaches the claimed invention as described above and furthermore, Ishimi teaches that said second operational mode is designated by a memory mode bit (DM bit of a BMC register 900) (e.g. se Col. 5, lines 5-11 and Fig. 3).

As per claim 10, Ishimi teaches the claimed invention as described above and furthermore, Ishimi teaches that the system further comprising: a device control register (the BMC register 900 in Fig. 3) storing said memory mode bit (e.g. se Col. 5, lines 5-11 and Fig. 3).

As per claim 1, Ishimi teaches a method of writing to cache comprising: initiating a write operation to a cache; in a first operational mode: detecting the presence or

absence of a write miss; if a write miss is absent, writing data to said cache; if a write miss is present, retrieving said data from a further memory and writing said data to said cache (e.g. see Col. 12, lines 40-43 and Col. 13, lines 24-32); in a second operational mode: placing said cache in a memory mode; writing said data to said cache regardless of whether a write miss is present or absent (e.g. see Col. 5, lines 14-17).

As per claims 2-3, see arguments with respect to the rejection of claims 9 and 10, respectively. Claims 2 and 3 are also rejected based on the same rationale as the rejection of claims 9 and 10, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-5, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi in view of Shah et al. (USPN: 4,604,727) hereinafter, Shah.

As per claim 11, Ishimi teaches the claimed invention as described above. However, Ishimi does not teach that the second operational mode is designated by address bits contained within said address. Shah, on the other hand, teaches that the second operational mode (i.e. write protect control mode) is designated by address bits (i.e. 3 most significant row address bits) contained within the address (e.g. see Col. 14, lines 47-59). Accordingly, it would have been obvious to one of ordinary skill in the art

at the time of the current invention was made to use the address bits of the address to designate the second operational mode as taught by Shah in the system taught by Ishimi. In doing so, just by examining the appropriate address bits of the address, the operational mode of the cache can be determined.

As per claim 12, the combination of Ishimi and Shah teaches the claimed invention as described above and furthermore, Shah teaches that said by address bits contained within said address include the high order address bits (e.g. see Col. 14, lines 47-59). Keeping high order address bits equal to '1111' for designating the second operational mode is a system dependent feature. Since neither applicant nor specification specifically disclose that using some other value other than '1111' in the high order address bits would change the system functionality or performance, therefore, any number of high order bits can be selected for setting to any specific value for designating the second operation mode.

As per claims 4-5, see arguments with respect to the rejection of claims 11 and 12, respectively. Claims 4 and 5 are also rejected based on the same rationale as the rejection of claims 11 and 12, respectively.

6. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi in view of Anthony et al. (USPN: 4,885,680) hereinafter, Anthony.

As per claim 14, Ishimi teaches the claimed invention as described above but failed to teach that the control logic invalidates cache directory entries associated with writing said data in response to a select all bins bit. However, Anthony teaches that

when the cacheability of the temporarily cacheable data changes from cacheable to non-cacheable, a single instruction is issued to cause the cache to invalidate all marked data. When an "invalidate marked data" (similar to the claimed "a select all bins bit") instruction is received, the cache controls sweep through the entire cache directory and invalidate any cache line that has the "marked data bit" set in a single pass (e.g. see the abstract and claim 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Anthony in Ishimi's system. In doing so, it improves system performance as result of reduced memory latency and improved coherence of data.

As per claim 7, see arguments with respect to the rejection of claim 14. Claim 7 is also rejected based on the same rationale as the rejection of claim 14.

7. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi.

As per claim 13, Ishimi teaches the claimed invention as described above but failed to teach that said control logic retrieves a bin identifier from said address, said bin identifier designating said compartment of said cache where said data is to be written, i.e. the control logic retrieves which cache line needs to be written/updated in the cache. However, many different cache replacement algorithms, such as LRU, MRU, FIFO, LIFO etc. the cache controller retrieves the cache location that needs to replaced, are well-known and notorious old in the art. The Examiner herein taking Official Notice on this subject matter.

As per claim 6, see arguments with respect to the rejection of claim 13. Claim 6 is also rejected based on the same rationale as the rejection of claim 13.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER